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# PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 8071-12 (OPP 011059US)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on November 23, 2005

Signature: David L. Heath

Typed or printed name: David L. Heath

| Application Number | Filed |
|---|---|
| 10/083,261 | February 25, 2002 |

First Named Inventor: Choi

| Art Unit | Examiner |
|---|---|
| 2871 | George Y. Wang |

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 46,763
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

David L. Heath
Signature

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516-692-8888
Telephone number

November 23, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Applicants: Choi, et al.

Examiner: George Y. Wang

Serial No: 10/083,261

Group Art Unit: 2871

Filed: February 25, 2002

Docket: 8071-12 (OPP 011059US)

For: **THIN FILM TRANSISTOR ARRAY SUBSTRATE USING LOW DIELECTRIC INSULATING LAYER AND METHOD OF FABRICATING THE SAME**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

## PRE-APPEAL BRIEF REQUEST FOR REVIEW

In response to the Advisory Action dated November 8, 2005, rejecting Claims 1-2, 7-12, and 33-40 under 35 U.S.C. §103, Applicant appeals pursuant to the Notice of Appeal filed herewith, and submits the following Pre-Appeal Brief Request for Review.

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CERTIFICATE OF MAILING 37 C.F.R. §1.8(a)

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Dated: 11/23/05 David L. Hecht

## ARGUMENTS

Claims 1-2, 7-12, and 33-40 are pending in this application. The Examiner has maintained the following section 103 obviousness rejections:

Claims 1, 7-9, and 11-12 over U.S. Patent No. 5,920,084 (Gu, *et al.*) in view of U.S. Patent No. 5,053,844 (Murakami, *et al.*);

Claims 33, 37, and 39-40 over Gu in view of U.S. Patent No. 5,646,756 (Dohjo, *et al.*) and U.S. Patent No. 5,668,379 (Ono, *et al.*);

Claims 2 and 34-36 over Gu, Murakami, Dohjo, and Ono;

and

Claims 10 and 38 over Gu, Murakami and Dohjo, Ono, and further in view of U.S. Patent No. 5,671,027 (Sasano, *et al.*).

Applicant's independent claim 1 is directed to a thin film transistor array substrate that includes a *second insulating layer is formed with an a-Si:C:O layer or an a-Si:O:F layer.* The Examiner conceded that Gu fails to disclose such a feature, and then cites Murakami as disclosing an insulating a-Si layer formed from a-Si:O:F. However, the Examiner has not established a proper motivation for combining Murakami with Gu.

Murakami does not suggest using this material in a thin film transistor since Murakami discloses a photosensor device, a device for detecting light. Applicant's claim 1 is directed to a *thin film transistor array substrate* which forms part of an LCD display, a device for emitting light, and a different technical field from that of photosensors. Murakami's photosensor includes three or four amorphous silicon layers. The materials used for Murakami's photosensor layers are chosen for specific bandgap properties to produce a sensor with a high Ip/Id ratio and applicable to sensing color. Murakami discloses the use of a-Si:O:F as a second end amorphous silicon layer, which has an optical band gap of 1.9 eV or more. Murakami applies the a-Si:O:F layer for adjusting an energy band gap between layers

of a photosensor. This is a different use of the a-Si:O:F layer from that of the present invention, wherein the a-Si:O:F layer is used due to its low dielectric constant for reducing cross-talk between the first pixel electrode and the second signal line. Furthermore, the Examiner asserted that the amorphous silicon layers of Murakami "reduce the band gap thickness, which ultimately increases the intensity ratio, improves uniformity in structure, and maximizes color-sensing application" are motivation to combine Murakami and Gu. These alleged advantages of Murakami are not relevant to an insulating layer of a thin film transistor array substrate, as an insulating layer does not require such conditions. The purpose of the a-Si:O:F insulating layer is to reduce or minimize parasitic capacitance between the first pixel electrode and the second signal line. One skilled in the art would not look to the teachings of Murakami for optimizing capacitance.

In addition, Applicant disagrees with the Examiner's allegation in the Final Office Action dated August 23, 2005 that recognizing another advantage that would flow from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. In particular, the Examiner stated that "[s]imply because Applicant has recognized that one purpose of the a-Si:O:F insulating layer is to reduce or minimize parasitic capacitance does not preclude such use of the insulating layer from advantages associated with reducing the band gap thickness . . . ." The Examiner's argument that recognizing the utility of an a-Si:O:F insulating layer to reduce parasitic capacitance does not preclude its use in reducing band gap thickness is irrelevant, since the issue is whether using a a-Si:O:F layer to reduce bad gap renders obvious its use to reduce capacitance. The advantages associated with reducing the band gap in a photo-sensor do not motivate applying an a-Si:O:F layer as a passivation layer of a thin film transistor array panel since reducing the band gap in a photo-sensor does not provide any advantage or effect for a passivation layer in a thin film transistor array panel. Applicant is not urging that patentability be admitted because Applicant has recognized another advantage of a-Si:O:F, but rather that there is no motivation to combine a-Si:O:F of Murakami's photo-sensor with a thin film transistor panel according the description of Gu.

Therefore, claim 1 is not *prima facie* obvious in view of Gu and Murakami, and this rejection under 35 USC 103 should be reversed.

Applicant's independent claim 33 is directed to a thin film transistor array substrate that includes *a second insulating layer having dielectric constant about 4.0 or less,* and a *first insulating layer[that] includes a top layer and a bottom layer, the bottom layer being an a-Si:O:F layer.* The Examiner conceded that Gu fails to disclose a bottom layer having a dielectric constant about 4.0 or less, but then cited Dohjo and Ono as disclosing these features. Once again, the Examiner has not established a proper motivation for combining Murakami with Dohjo and Ono.

The Examiner asserted that ref. 16 of Fig. 1 of Dohjo corresponds to the bottom layer of the insulating layer, while Fig. 1, ref. 20 of Dohjo corresponds to the top layer. However, there is no ref. 16 in Dohjo's Fig. 1, and the ref. 16 disclosed in Dohjo refers instead to semiconductor layer in Figs. 5 and 6, not an insulating layer (see Col. 7, lines 27-35). A semi-conductor layer is different from an insulating layer. Furthermore, the section of Dohjo that describes ref. 20 of Fig. 1, col. 7, lines 41-45, describes it as a signal line that functions as a source electrode and a drain electrode. A signal line functioning as an electrode is different from an insulating layer. In addition, Ono does not rectify these deficiencies in Dohjo.

In addition, the Examiner argues that "nowhere in the claim does it specify that the bottom layer [of the first insulating layer] must be an insulating layer." Applicant disagrees, and pints out that by reciting that *the first insulating layer includes a top layer and a bottom layer*, the claim is specifying that the bottom layer is an insulating layer. Furthermore, Applicant does not agree with the Examiner's statement that "even a semi-conductor layer can function to 'insulate' one portion of the array with another", as by that interpretation any layer in a TFT array can serve that purpose. However, a semi-conductor layer will not in general serve to electrically insulate one layer from another, and does not serve that purpose in Dohjo, since Dohjo specifically discloses insulating layers 14 and 15 that serve that purpose. Thus, Dohjo does not disclose or suggest *a first insulating layer includes a top*

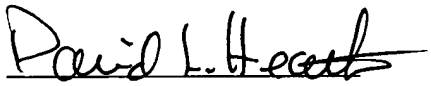
*layer and a bottom layer, the bottom layer being an a-Si:O:F layer, and the top layer being a silicon nitride layer,* as recited in claim 33.

Claim 33 was amended in the Response dated October 24, 2005, to recite "the bottom layer being an a-Si:O:F layer", a feature previously recited in claim 34. The Examiner cited Ono for disclosing a substrate with a dielectric constant about 4 or less. However, the passage of Ono cited by the Examiner discloses either an $SiO_2$ film, or a film made of two layers of $SiO_2$ and SiN. Ono does not disclose or suggest a film having a *bottom layer being an a-Si:O:F layer.*

Thus, Applicant urges that the combination of Gu, Dohjo, and Ono do not teach or suggest all of the claimed features of claim 33, and that a *prima facie* case of obviousness of claim 33 over the combination of Gu, Dohjo, and Ono cannot be maintained. This rejection should be reversed.

Claims 2 and 7-12 depend from claim 1, and are thus patentable for at least the same reasons as claim 1. Claims 35-40 depend from claim 33, and are thus patentable for at least the same reasons as claim 33. Accordingly, these rejections should be reversed.

Respectfully submitted,

By: 

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